A Scalar Resonant-Filter-Bank-Based Output-Voltage Control Method and a Scalar Minimum-Switching-Loss Discontinuous PWM Method for the Four-Leg-Inverter-Based Three-Phase Four-Wire Power Supply

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***Abstract*—An all-scalar-control and pulsewidth-modulation (PWM) approach for the four-leg-inverter (FLI)-based three-phase transformerless four-wire power supply (PS) is proposed. The output voltage of each phase is controlled independently, and its controller is formed by a stationary-frame resonant-filter bank accompanied with proportional-control and output-capacitor current-based active-damping loops. The simple and easy to implement scalar-control method exhibits superior overall steady-state and dynamic performance in the PS applications involving loads with high crest factor and/or significant load imbalance. Utilizing the inverter zero-state partitioning, a generalized form of scalar PWM for the FLI is developed. A novel minimum loss discontinuous PWM method, which provides minimum switching losses under all loading conditions (including load imbalance), is derived. This simple scalar method provides superior performance, and unlike the vector methods, it is easy to implement. The controller and modulator design and implementation details for the system are given. Linear and nonlinear loads for balanced and imbalanced load operating conditions are considered. The scalar-control and PWM methods are proven by means of theory, simulations, and thorough laboratory experiments of a 5-kVA PS.**

***Index Terms*—Active damping, control, crest factor, discontinuous PWM (DPWM), four-leg, four-wire, harmonic, imbalance, inverter, minimum loss discontinuous PWM (MLDPWM), minimum switching loss, power supply (PS), pulsewidth modulation (PWM), resonant-filter controller, scalar, three-phase, voltage regulation.**

I. Introduction

THE CONVENTIONAL method of making a dc/ac three-phase four-wire power supply (PS) by means of an inverter involves the utilization of a Δ/Y or Δ/Z winding transformer between the standard three-leg inverter and the load. The star point of the transformer, which forms the neutral point of the supply, provides the path for the zero-sequence component of the load currents which may occur due to single-phase loading, load imbalance, and/or harmonics. With the transformer being bulky and expensive, the modern approach to making a three-phase four-wire PS involves transformerless power converter configurations [1]–[3]. Of the two favorable inverter topologies, the conventional half-bridge topology (most widely utilized) involves three inverter legs and utilizes the dc-bus midpoint as neutral point terminal [3]. Although its structure is simple, the half-bridge topology has poor dc-bus voltage utilization and requires a large dc-bus voltage in order to obtain the required output voltage. Furthermore, under load-current imbalances and/or harmonics, the neutral wire current loads the dc-bus capacitor and causes oscillation/drift of the neutral point potential. This problem is avoided by utilizing large dc-bus capacitors and dc-bus capacitor voltage balancing mechanisms [3]. The less popular, but higher performance, topology is the four-leg voltage-source inverter (FLI) topology [1], [4]–[9].

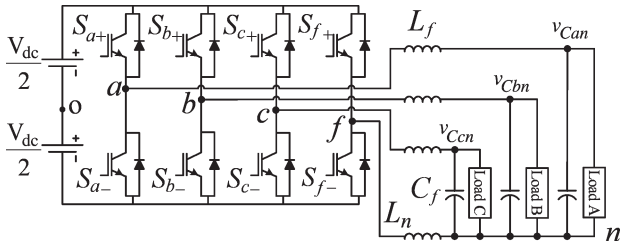

Fig. 1. Three-phase FLI-PS system basic circuit configuration.

As shown in Fig. 1, the FLI-PS topology involves an additional leg compared to the conventional three-leg inverter such that the fourth leg provides a path for the zero-sequence currents of nonlinear and imbalanced loads. Since there is no dc-bus midpoint connection to the load and the load-current zero-sequence component is circulated in the system via the fourth leg (unlike the three-leg half-bridge inverter with dc-bus midpoint connection), the dc-bus capacitor size and the dc-bus voltage oscillations can be made small [1], [5]. Furthermore, the dc-bus voltage utilization of the FLI topology is better, and to obtain a specific output voltage, a lower dc-bus voltage than the half-bridge topology suffices (15% less dc-bus voltage

Paper 2008-IPCC-055, presented at the 2007 IEEE International Electric Machines and Drives Conference, Antalya, Turkey, May 3–5, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Power Converter Committee of the IEEE Industry Applications Society. Manuscript submitted for review May 12, 2008 and released for publication October 3, 2008. Current version published May 20, 2009.

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Digital Object Identifier 10.1109/TIA.2009.2018980

for the same output voltage under the assumption of balanced operating condition). This implies less electromagnetic stresses and less switching losses in the converter [1], [5]. Since it involves three independent load phases and four inverter legs (two additional switches and $2^4 = 16$ switch states), the FLI structure is more complex than the classical half-bridge three-leg inverter. Therefore, its control and pulsewidth modulation (PWM) methods have been considered as complex from the learning, controller design, and implementation perspectives. As a result, the FLI-PS topology has found limited practical applications until recently [1].

Output-voltage control of an FLI-PS typically involves classical linear regulators (stationary/synchronous frame PID) [4]–[9] or modern control methods such as deadbeat and predictive control. In the classical stationary-/synchronous-frame control methods, the three-phase variables are coordinate transformed to the control coordinates ($\alpha\beta 0$ and/or $dq0$). The controller operates on the error, and the manipulation signals are obtained. Then, an inverse transformation is employed, and the PWM signals are applied to the FLI. In the synchronous-frame approach, the dq variables are controlled with linear PI regulators, while the zero-sequence component is separately controlled with a different type controller [7]–[9]. As a result, a complex controller structure and/or poor performance become inevitable [4]–[13]. Predictive and deadbeat controllers require accurate system parameter knowledge which is frequently not available.

Similar to the control issues, the PWM pulse-pattern determination process of FLI is also difficult and complex. The 3-D space vector PWM (3-D-SVPWM) approach involves a complex procedure (defining a region among 24, the sequence for five vectors, and converting vector duty cycles to switch duty cycles) that is time consuming and nonintuitive [5], [9], [14]–[17]. Although, with proper algorithms, the 3-D-SVPWM can be utilized to generate high-performance pulse patterns, due to its complexity, the method is not favorable. The scalar PWM method, which has been developed for the FLI [18], [19], is easier to implement; however, it is not well established. The relation between the space vector approach and scalar approach has not been clearly defined. Switching-loss optimal switching patterns considering the imbalanced load operating conditions of the FLI-PS have not been reported yet.

This paper proposes simple and easy to implement, yet highly performing, scalar-control and PWM methods for the FLI-PS. In this all-scalar-control and PWM approach, the output voltage of each phase is controlled independently, and its controller is formed by a stationary-frame resonant-filter bank [20]–[27] accompanied with proportional-control, output-capacitor current-based active-damping [28], and command voltage feedforward loops. The simple and easy to implement scalar-control method yields superior overall steady-state and dynamic performance in the FLI-PS application. Utilizing the inverter zero-state partitioning, a generalized form of scalar PWM for the FLI is developed, and a novel minimum loss discontinuous PWM (MLDPWM) method, which provides minimum switching loss under all operating conditions (including imbalanced load operation), is proposed [29]. Since the FLI topology is suitable for imbalanced load operating conditions, the MLDPWM method is suitable for the FLI and, specifically, for the FLI-PS application. This simple scalar method provides superior performance, and unlike the vector methods, it is easy to implement. With the proposed approach, the seemingly complex FLI-PS system becomes easy to manipulate, thus becoming favorable over the half-bridge topology.

This paper first discusses the scalar controller. Second, the scalar PWM approach is described in detail. The controller and modulator design and implementation details are provided. Then, detailed FLI-PS system simulations are followed by experimental studies of a 5-kVA system. Linear and nonlinear loads for balanced and imbalanced load operating conditions are considered. Theory, simulation, and experimental studies are all correlated, and the high performance of the proposed methods is demonstrated.

II. Control of FLI-PS Output Voltages

A. Selection of the Controller Type

The FLI topology allows one to control all the three-phase variables independently. Thus, the output voltages of the three-phase FLI-PS can be controlled independently. The conventional approach of decomposing the abc phase variables to the stationary-frame $\alpha\beta 0$ and then to the synchronous-frame $dq0$ variables and performing the control action in rotating complex coordinates involves difficulties. While the positive- and negative-sequence components can be manipulated with linear PID controllers (and cross-coupling decoupling) in the synchronously rotating frames [12], [13], the zero-sequence component requires a stationary frame controller of different type, which complicates the design and is typically of a low bandwidth [7], [8]. Thus, low-bandwidth output-voltage control results. Instead of the decomposition approach, the recently developed resonant-filter-bank control approach can be utilized to directly control the three-phase abc variables of the FLI-PS system. Since the variables are directly manipulated in the stationary frame (no vector transformations), this approach is termed as "scalar control," and it is favored in this paper due to its simplicity, ease of implementation, and intuitive nature.

Since the PS requires high-bandwidth output-voltage control, scalar control of the output voltages cannot be performed by simple PID-type controllers. As the command frequency and load harmonic frequencies are well defined in this application, it is possible to employ the resonant-filter control approach which provides very high gain at a desired resonant frequency and zero gain elsewhere [20]–[27]. However, for each frequency of interest, one controller becomes necessary. With high-performance DSP systems, implementing such resonant-filter-bank controllers is presently viable [23], [27]. Thus, in this paper, the resonant-filter control approach will be employed. For each phase of the FLI-PS, one identical resonant-filter-bank controller is utilized and acts on the output-voltage error of the associated FLI-PS phase. Each resonant-filter bank includes a fundamental-frequency resonant-filter controller and a set of harmonic-frequency resonant-filter controllers. In addition to the resonant-filter bank, each phase involves a proportional controller acting on the output-voltage error for the purpose of improving the output-voltage dynamic response. Thus, the total controller is termed as P+Resonant controller, and its

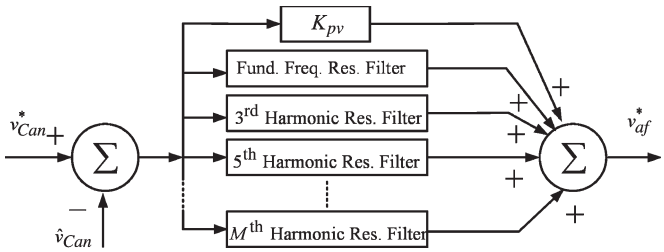

Fig. 2. Per-phase P+resonant-filter-bank controller structure.

structure is shown in Fig. 2, where M, the order of the resonant-filter bank, indicates the highest harmonic frequency that the resonant filters can control.

B. Resonant-Filter-Bank Controller Design

Proper design of the resonant-filter banks requires the knowledge of the implementation platform (fixed versus floating point DSP), PS output frequency tolerance range, and the resonant frequency of the PS output LC filter. Given this information, the filter selectivity and phase advance for each resonant frequency are calculated, and the control algorithm is implemented.

The gain of the loss-less resonant filter at the resonant frequency is very high, and the sidebands are very small. This implies that the controller is highly selective and can only track a reference exactly at the designed value of $m\omega_e$ the resonant frequency considered $(m = 1, 3, 5, 7, \ldots, M)$. In practice, if the resonant-filter controller is implemented with a fixed-point DSP, the filter coefficients are represented with finite word length, and loss of significance occurs. As a result, the phase and magnitude of the practical resonant filter become significantly different from the theoretical values. The gain significantly decreases, and the phase angle deviates from zero. The end result is poor output-voltage controller performance. To avoid this problem, the sharp filter gain characteristic is smoothened, and the selectivity of the filter S which is defined in (1) [30] is decreased, and its damping ζ_m defined in (2) is increased [22], [23]

$$S = \frac{\text{resonant frequency}}{\text{bandwidth}} = \frac{m\omega_e}{\Delta\omega} \tag{1}$$

$$\zeta_m = \Delta\omega/(2m\omega_e). \tag{2}$$

In (1) and (2), m, ω_e, and $\Delta\omega$ correspond to the order of the harmonic frequency, fundamental frequency, and the bandwidth of the resonant frequency, respectively. Fig. 3 assists in describing the gain characteristic of the flattened response resonant filter where K_{im} corresponds to the maximum gain of the filter at the resonant frequency.

The second important design consideration of the resonant-filter controllers involves the phase-angle compensation for the purpose of stability enhancement [7], [23]. Practically, the measurement, DSP, and inverter units introduce delays that can have significant influence on the controller performance, particularly at the high-frequency range (as the LC filter resonant frequency is approached). The phase shift due to these delays, i.e., ϕ_m, increases with the frequency and can be obtained as a function of the total system delay and the resonant frequency $(m\omega_e)$ of

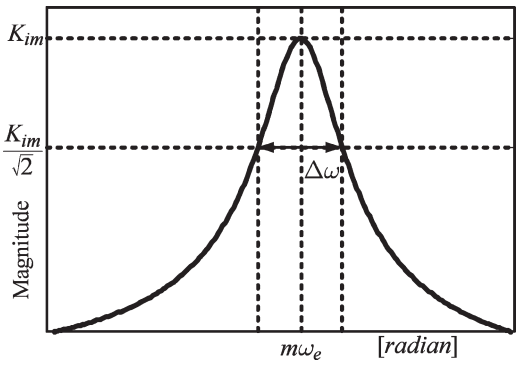

Fig. 3. Gain characteristic of a damped resonant filter.

the controller, as given in (3) where τ_T is the total system delay (typically two PWM cycles) [23]

$$\phi_m = \tau_T \cdot m\omega_e. \tag{3}$$

Additional phase advancing may be required as the resonant frequency of the LC filter of the PS is approached in order to compensate for the significant phase lag of the LC filter near its resonant frequency. Since the phase shift is proportional to the frequency, its influence is significant at the high-frequency range, while it can be ignored at low frequency.

Following the design guidelines given, when the resonant-filter bank is implemented and the proportional gain controller K_{pv} is included, the general feedback controller transfer function of (4) is obtained

$$G_C(s) = K_{\text{pv}} + \sum_{\substack{m=1 \\ m\ \text{odd}}}^{M} \frac{2K_{\text{im}} \cdot \zeta_m m\omega_e \left(s\cos(\phi_m) - m\omega_e \sin(\phi_m)\right)}{s^2 + 2\zeta_m m\omega_e s + (m\omega_e)^2}. \tag{4}$$

For $m = 1$, the fundamental-frequency (ω_e) controller provides fundamental-component (positive-sequence) voltage regulation. The resonant-filter-bank harmonic-frequency controllers of the FLI-PS are selected such that the dominant current harmonics of the nonlinear load (3rd, 5th, 7th harmonic, etc.) are manipulated by the resonant-filter bank and the output voltage is free of these harmonics. Depending on the DSP capability and measurement resolution, compensation up to high degree of harmonics may be achieved. In the literature, compensation up to the 29th harmonic has been reported [27].

In Figs. 4 and 5, illustrative examples of the resonant-filter controller magnitude and phase characteristics are shown. Fig. 4 shows the fundamental-frequency resonant-filter controller gain and phase characteristics, while Fig. 5 shows the total controller characteristics including the fundamental and the first six dominant harmonics. It is apparent from these characteristics that the controllers will regulate the output-voltage fundamental component with high accuracy and suppress all the dominant harmonic voltages significantly.

The resonant-filter-bank controller provides superior steady-state performance and good dynamic performance within a bandwidth, including the highest resonant-filter controller frequency. However, its dynamic response is limited, and the proportional gain alone cannot improve the dynamic response

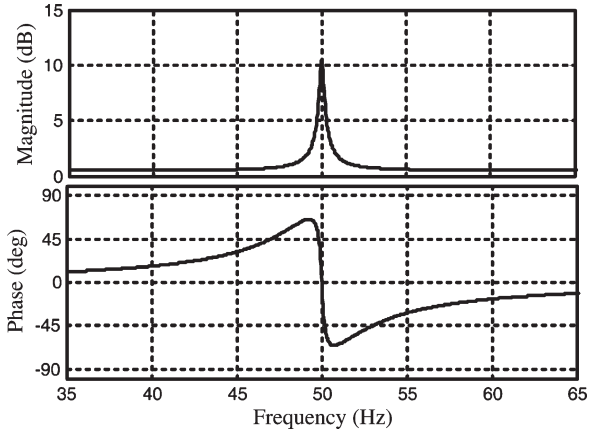

Fig. 4. Gain and phase characteristics of the damped P+resonant-filter controller for $K_{\rm pv} = 0.5$, $m = 1$, $K_{i1} = 10$, $\omega_e = 2\pi 50$ rad/s, $\zeta_1 = 3.18 \times 10^{-3}$, and $S = 100\pi$ ($\Delta f = \Delta\omega/2\pi = 0.16$ Hz).

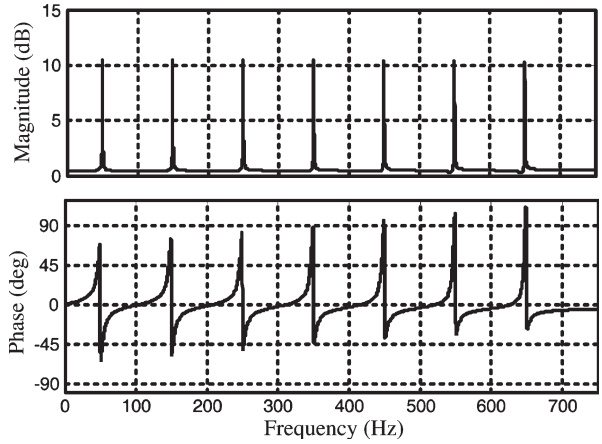

Fig. 5. Gain and phase characteristics of the phase compensated and damped P+resonant-filter bank for $m = \{1, 3, 5, 7, 9, 11, 13\}$, $K_{\rm pv} = 0.5$, $K_{\rm im} = 10$, $\omega_e = 2\pi 50$ rad/s, $\zeta_m = 3.18 \times 10^{-3}$, $S = 100\pi$ ($\Delta f = 0.16$ Hz), and $\phi_m = 2T_s \cdot m\omega_e$.

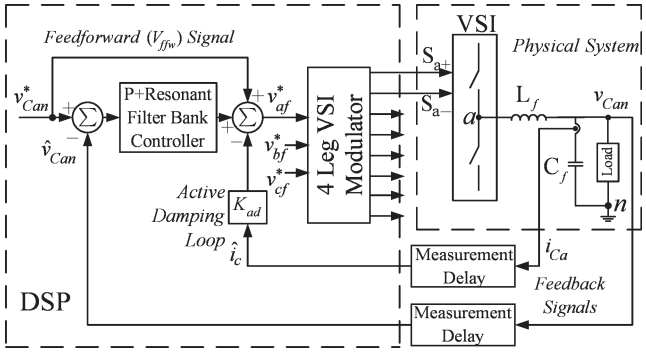

Fig. 6. Control system block diagram of the FLI-PS system.

of the controller under step load changes. In order to obtain high dynamic performance, the output-capacitor current feedback loop (with a $K_{\rm ad}$ gain), which provides active damping and improves the load disturbance rejection characteristic [28], is added to the resonant filter. In addition, voltage feedforward is added to the controller for the purpose of good command tracking. Thus, the multiloop controller structure in Fig. 6 is obtained. For each phase, the controller operates on the output-voltage error, and the inverter phase voltage references v^*_{af}, v^*_{bf}, v^*_{cf} are obtained.

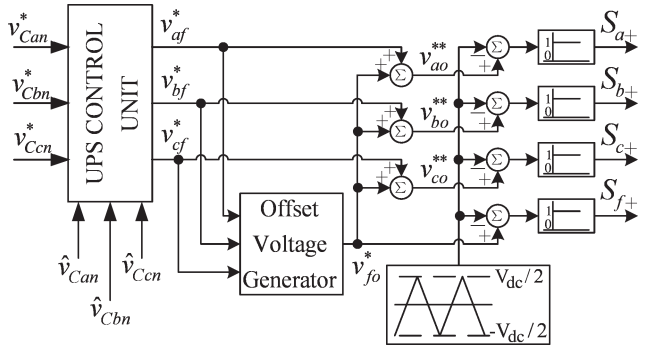

Fig. 7. Block diagram of the scalar modulation in FLI.

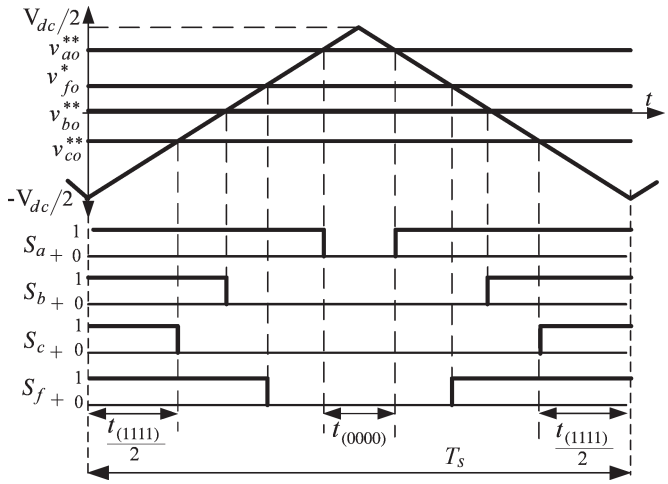

Fig. 8. Modulation and carrier signals and switching diagram of the FLI with $v^*_{fo} > 0$ illustrating the influence of v^*_{fo} on the width of the two zero states.

The stationary-frame resonant-filter-bank control approach provides an easy design and implementation task with respect to the synchronous-frame-based controller or other complex control algorithms. There is no need for involved $\alpha\beta 0$ and/or $dq0$ transformations, positive-/negative-/zero-sequence decomposition, and complex control structures. Thus, it is favored over other controller structures mentioned in this paper.

III. Scalar PWM for the FLI-PS

In the FLI-PS, the output-voltage controller generates the voltage references v^*_{af}, v^*_{bf}, v^*_{cf} for the three phases, all with respect to "f," the center point of the fourth leg. It is required to define the fourth-leg reference voltage v^*_{fo}. Then, all the inverter phase output terminal reference voltages $(v^{**}_{ao}, v^{**}_{bo}, v^{**}_{co})$ with respect to the virtual dc-bus midpoint are defined in (5)

$$v^{**}_{xo} = v^*_{xf} + v^*_{fo}, \qquad x \in \{a, b, c\}. \tag{5}$$

The next step is to generate the PWM output signals as in the three-leg inverter case [18], [19], [29], [31], [32]. Comparing the modulation signals with the triangular carrier wave, the intersections define the switching instants. Figs. 7 and 8 aid in illustrating the pulse-pattern generation method.

A. Offset Voltage Generation Methods

Since the center point of the dc-bus voltage is isolated and there is no path for current flow from the "f" point to the "o" point (see Fig. 1), there exists a degree of freedom in the choice of the v^*_{fo} value. Thus, this degree of freedom can be utilized to the advantage of the inverter in terms of performance optimization. As it is added to the original reference voltages v^*_{af}, v^*_{bf}, v^*_{cf} to obtain the inverter leg modulation signals, this signal is called the offset [18], [19] or injection signal [31], [32] (Fig. 7). Output current ripple minimization, voltage linearity range maximization, switching-loss minimization, etc., criteria can be utilized for optimization of the offset signal. To retain modulator voltage linearity, the modified reference voltages v^{**}_{ao}, v^{**}_{bo}, v^{**}_{co}, v^*_{fo} should be bounded with $\pm V_{\rm dc}/2$. As a result, the potential difference between any two inverter output terminals is bounded by $\pm V_{\rm dc}$.

There is a further constraint on v^*_{fo}, which will be discussed in the following. Of the three reference signals v^*_{af}, v^*_{bf}, v^*_{cf}, let us assume that the two extreme signals are $v^*_{\max}$ and $v^*_{\min}$ as defined in (6) and (7), respectively,

$$v^*_{\max} = \max\left(v^*_{af}, v^*_{bf}, v^*_{cf}\right) \tag{6}$$

$$v^*_{\min} = \min\left(v^*_{af}, v^*_{bf}, v^*_{cf}\right). \tag{7}$$

The largest possible v^*_{fo} that retains the system linearity is a function of the absolute value of $v^*_{\max} - v^*_{\min}$. If $v^*_{\max} - v^*_{\min}$ is smaller than $V_{\rm dc}$, there is a room for injecting a nonzero v^*_{fo}. The available range for the injection depends on the sign and magnitude of $v^*_{\max}$ and $v^*_{\min}$. The top and bottom limits of v^*_{fo} are given in (8) and (9)

$$v^*_{fo\_\rm top} = \begin{cases} V_{\rm dc}/2, & v^*_{\max} < 0 \\ V_{\rm dc}/2 - v^*_{\max}, & \text{elsewhere} \end{cases} \tag{8}$$

$$v^*_{fo\_\rm bottom} = \begin{cases} -V_{\rm dc}/2, & v^*_{\min} > 0 \\ -V_{\rm dc}/2 - v^*_{\min}, & \text{elsewhere.} \end{cases} \tag{9}$$

Depending on the top and bottom limit values of v^*_{fo}, a wide range may exist for the purpose of performance optimization. If no offset signal is injected, $v^*_{fo} = 0$ (the fourth leg is operated at 50% duty cycle), then $v^*_{af} = v^{**}_{ao}$, etc. If v^*_{fo} is selected within the boundaries of (8) and (9), all the original modulation signals of Fig. 8 simultaneously shift upward or downward, depending on the injection signal polarity. The intersection points of the reference signal with the carrier wave and thus the switching instants change. However, the modified signals v^{**}_{af}, v^{**}_{bf}, v^{**}_{cf} remain relatively at the same distance from each other. Thus, the widths of the rectangular line-to-line voltage pulses (and their average values) remain the same. Fig. 8 shows that this vertical movement changes the duration ratio of the inverter zero states 0000 and 1111. Defining the two zero states as $V_{(0000)}$ and $V_{(1111)}$ (which correspond to the zero voltage vectors of the space vector method defined in [5] and [9]) and their durations as $t_{(0000)}$ and $t_{(1111)}$, respectively (Fig. 8), the zero-state partitioning function ξ can be formulated in (10)

$$\xi = t_{(0000)} / \left(t_{(0000)} + t_{(1111)}\right). \tag{10}$$

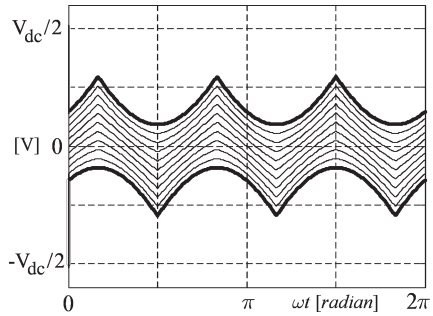

Fig. 9. Injection signal waveforms within the $v^*_{fo\_\rm top}$ and $v^*_{fo\_\rm bottom}$ boundaries as a function of ξ for $M_i = 0.64$ (ξ is incremented from 0 to 1 by 0.1).

ξ has a range between 0 and 1. As v^*_{fo} increases, ξ linearly decreases. Involving (8) and (9), the relation between ξ and v^*_{fo} can be written in (11), or as a function of $v^*_{\max}$ and $v^*_{\min}$, it can be written in (12) [29]

$$v^*_{fo} = (1-\xi)\left(v^*_{fo\_\rm top}\right) + \xi\left(v^*_{fo\_\rm bottom}\right) \tag{11}$$

$$v^*_{fo} = \begin{cases} (1/2-\xi)V_{\rm dc} - \xi v^*_{\min}, & v^*_{\max} < 0 \\ (1/2-\xi)V_{\rm dc} + (\xi-1)v^*_{\max}, & v^*_{\min} > 0 \\ (1/2-\xi)V_{\rm dc} + (\xi-1)v^*_{\max} - \xi v^*_{\min}, & \text{elsewhere.} \end{cases} \tag{12}$$

In order to illustrate the ξ and v^*_{fo} relations, operation at the modulation index (M_i) value of 0.64 is considered. M_i is defined as $M_i = 0.5\,\pi V_{1m}/V_{\rm dc}$, where V_{1m} is the fundamental-component magnitude of the line-to-neutral inverter output voltage. As shown in Fig. 9, as ξ is incremented with 0.1 steps from 0 to 1, the offset signal v^*_{fo} decreases from $v^*_{fo\_\rm top}$ to $v^*_{fo\_\rm bottom}$. As M_i increases, the two boundaries approach each other, and the range for v^*_{fo} expires (in the space vector illustration, the inverter hexagonal prism boundaries are reached [29]). Between the two boundaries, the range of v^*_{fo} (or ξ) can be utilized to optimize a specific performance of the modulator. As a result, various PWM schemes arise. The ξ-based modulation signal definition approach of (12) allows the unification of all the scalar PWM methods for FLI under one umbrella as previously established for the three-leg inverter [32]. The PWM methods discussed in the following are defined by the ξ function. Since SVPWM [33] assumes equal zero-state partitioning, by definition, $\xi_{\rm SVPWM} = 0.5$, which is the same as in the three-leg inverter case. The DPWM1 method [34], which is widely utilized in the three-leg inverter and specifically at high M_i due to its low output-voltage ripple and reduced switching losses, involves locking the phase with the largest magnitude to the same side of the dc-bus of the inverter. This method can be applied to FLI, and for this inverter, the ξ of DPWM1 is given in (13)

$$\xi_{\rm DPWM1} = \begin{cases} 0, & \left|v^*_{fo\_\rm top}\right| > \left|v^*_{fo\_\rm bottom}\right| \\ 1, & \left|v^*_{fo\_\rm top}\right| < \left|v^*_{fo\_\rm bottom}\right| \end{cases}. \tag{13}$$

TABLE I
SYSTEM PARAMETERS

Inverter	DC bus voltage (V_{dc})	540 V
	Switching frequency (f_{sw})	20 kHz
	Sampling frequency (f_s)	20 kHz
Filter	Inductor (L_f)	1.5 mH
	Capacitor (C_f)	30 μF
	Fourth leg inductor (L_n)	500 μH

B. The MLDPWM Method

Although the DPWM1 method and, in a more generalized form, GPDPWM [34] provide switching-loss reduction within a specific power factor range, they are inadequate for the FLI-PS under load unbalance. For this purpose, the following new method is proposed for the PS applications. In the MLDPWM method [29], the offset signal is determined by considering both the largest phase magnitude voltages and the currents associated with these phases. Of $v^*_{\max}$ and $v^*_{\min}$, the one that carries larger current is selected. This leg is clamped to the closer dc rail side, while all other legs are shifted by the same amount in the same direction. With this choice, the switching losses are minimized because the inverter leg that carries the largest current is not switched (of the two alternatives, the leg with the smaller current is switched) [34], [35]. For MLDPWM, ξ is given in (14),

$$\xi_{\mathrm{MLDPWM}} = \begin{cases} 0, & |I_{v\max}| > |I_{v\min}| \\ 1, & |I_{v\max}| < |I_{v\min}| \end{cases} \tag{14}$$

where $I_{v\max}$ and $I_{v\min}$ are the phase current magnitudes of $v^*_{\max}$ and $v^*_{\min}$, respectively. Similar to other DPWM methods, MLDPWM exhibits low PWM ripple at high M_i and is suitable for PS applications involving load imbalance.

C. Practical Implementation

The practical implementation of the discussed scalar PWM methods involves simple comparisons and computations. v^*_{af}, v^*_{bf}, v^*_{cf} and, if necessary, the inverter currents are evaluated by simple comparisons. Based on the results, the modulation signals are obtained by simple computations. For example, for SVPWM, $v^*_{fo} = -0.5\,(v^*_{\max} + v^*_{\min})$, and then employing (5), the final modulation signals are obtained. For MLDPWM, both the voltage references and phase current magnitudes are taken into consideration. First, (6) and (7) are evaluated. The currents of the extremum voltages define ξ as given in (14). At the final stage, v^*_{fo} is calculated from (12) and injected as in (5).

IV. COMPUTER SIMULATIONS

In this section, the performances of the proposed control and PWM methods for the FLI-PS are investigated by means of computer simulations using Ansoft-Simplorer where the inverter is fully modeled and the control system is implemented in discrete time. A 5-kVA 120-V_{rms}/phase 50-Hz FLI-PS is considered. The filter parameters, dc-bus voltage, and switching/sampling frequency are given in Table I. For the balanced load tests, resistive load (Y-connected, 8.4 Ω/phase) and, as a nonlinear load, a three-phase diode rectifier with RC load (24 Ω, 1.1 mF) are considered.

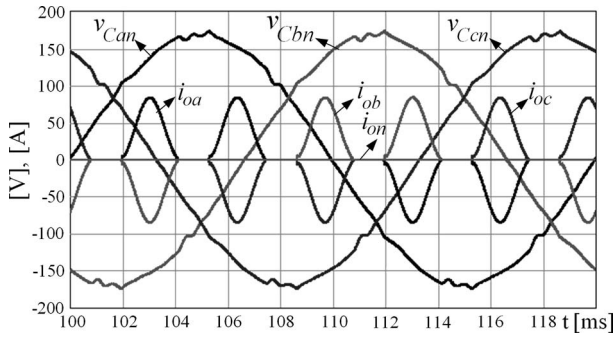

Fig. 10. Three-phase output voltages and load currents (scale: ×2.5) for closed-loop operation under balanced nonlinear rated load.

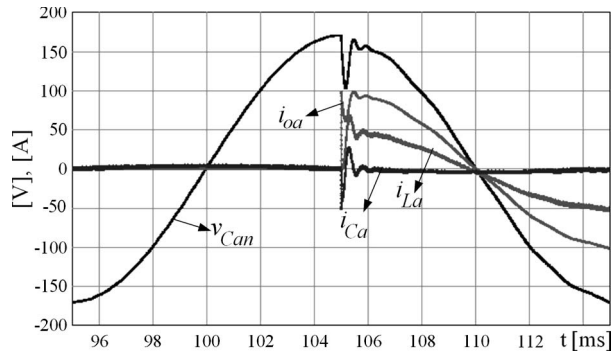

Fig. 11. Output phase voltage, load current (scale: ×5), inductor current (scale: ×2.5), and capacitor current (scale: ×2.5) waveforms of the closed-loop-controlled PS during loading transient.

A. Steady-State and Dynamic Performance

Fig. 10 shows the FLI-PS performance under nonlinear balanced rated load. With the closed-loop controller being active, VR, THD_V, and CF are 0.1%, 1.58%, and 2.45, respectively, compared to those of the open-loop controller with 4.8%, 12.2%, and 1.6, respectively. The fundamental-frequency controller regulates the output voltage with high accuracy, and the harmonic controllers lower the PS output impedance significantly such that THD_V is quite low. With the PS acting as an ideal voltage source, the nonlinear load-current crest factor becomes large compared to the open-loop-controlled case.

The dynamic performance of the PS is tested under balanced resistive rated load. The load is turned on at the peak of the PS phase output voltage, and a sag condition is generated. The voltage dip, settling time, and the lost volt–seconds are measured. Both open- and closed-loop tests are conducted, and those of the latter are shown in Fig. 11. The closed-loop-controlled FLI-PS output-voltage dip is 67 V, the settling time is 0.55 ms, and the lost volt–seconds are 19 mV · s, compared to those of open-loop, which are 85 V, 1.2 ms, and 55 mV · s, respectively. The active-damping loop improves the dynamic response significantly as the figure shows. The total delay time (from the instant of loading to the voltage dip point in Fig. 11) is approximately $2T_s$, which is the total system delay time.

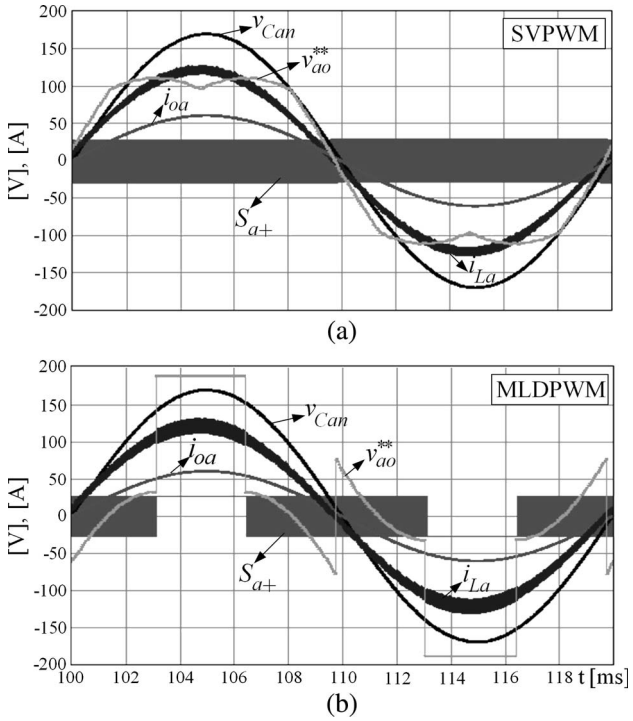

Fig. 12. Output voltage, modulation and switch logic signals, load current (scale: ×3), and inductor current (scale: ×6) under linear balanced load.

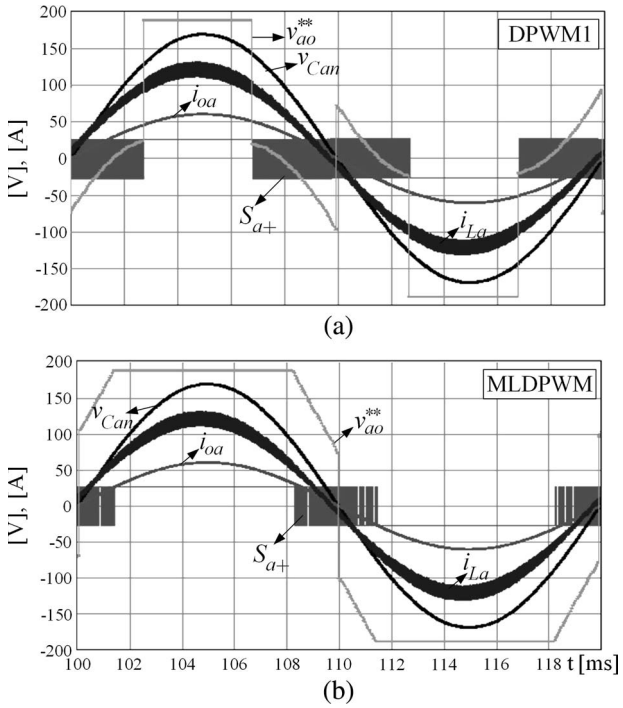

Fig. 13. Output voltage, modulation/switch logic signals, load current (scale: ×3), and inductor current (scale: ×6) under linear line-to-neutral imbalanced load.

B. Modulator Performance

For balanced, resistive rated-load, closed-loop, and steady-state operation, the inverter and load current, the output voltage, and the modulation/switch logic signal waveforms are shown in Fig. 12 for SVPWM and MLDPWM (same as DPWM1). Both PWM methods operate at 20 kHz. As in the three-leg inverter, smaller PWM current ripple favors SVPWM, and lower switching count and losses (25% less switching count and 50% less switching losses) favor MLDPWM. SVPWM characteristics are independent of the load. Although MLDPWM and DPWM1 exhibit the same performance for balanced linear load, their performances under nonlinear and/or imbalanced load differ. For linear resistive line-to-neutral imbalanced rated load, MLDPWM and DPWM1 method waveforms are shown in Fig. 13. For MLDPWM, switchings of the loaded phase cease for longer duration than 120°. Thus, switching losses decrease compared to DPWM1 (25.2% less) [29]. In this region, the loaded-phase PWM current ripple of MLDPWM is slightly higher than that of DPWM1. As shown in Fig. 14, the line-to-neutral imbalanced load current flows through the loaded phase and the fourth leg, while the unloaded phases carry small amount of current. As a result, MLDPWM respects the load-current information (similar to GDPWM of three-leg inverter [34]) in addition to the reference-voltage magnitude information such that the switches of the phase with the largest current are selected to be locked to the dc rail for longer time intervals than the DPWM1 case, yielding lower switching losses. In this discussion, the switching-loss calculation is based on the assumption that the switching devices have linear current turn-on and turn-off characteristics [32]. In modern practical devices (IGBTs, power MOSFETs, etc.), the switching characteristics deviate from the linear approximation, more or less depending on the device type. However, all device datasheets indicate that switching losses are proportional to the current magnitude. Based on this fact, it can be stated that, although the relative switching-loss comparison among methods is not easy to determine by experiments or modeling, it is clear that MLDPWM has the lowest losses. In previous studies, it has been shown that employing a PWM method that is locking the inverter phase leg with largest current leads to less temperature rise [34] and less total inverter losses [35] compared to other PWM methods.

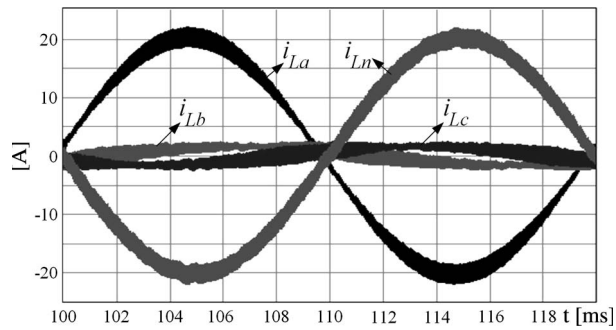

Fig. 14. Steady-state inverter output currents of MLDPWM under resistive line-to-neutral imbalanced load.

V. Experimental Results

In this section, the performances of the proposed control and PWM methods for the FLI-PS are investigated by laboratory experiments. An FLI-PS with the same ratings as the simulated system has been built and tested in the laboratory. The PS is controlled by a DSP (TMS320F2812). The experimental system parameters are the same as those in Table I. The same controller design, tuning, and the FLI-PS performance test steps as those of the simulations are followed in the laboratory.

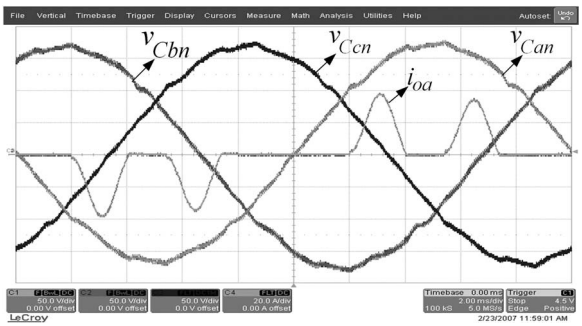

Fig. 15. Output voltages and one phase load current for closed-loop operation under balanced nonlinear rated load (scales: 50 V/div, 20 A/div, 2 ms/div).

TABLE II
EXPERIMENTAL STEADY-STATE PERFORMANCE OF THE FLI-PS AT VARIOUS LOAD CONDITIONS

		Linear load		Nonlinear load	
		Open-loop	*Closed-loop*	*Open-loop*	*Closed-loop*
Balanced load	CF	1.43	1.44	1.65	2.60
	VR (%)	14.95	0.33~0.45	13.63	0.16~0.33
	THD_V (%)	4.6	0.7	10.6	1.8
	V_{neg} (%)	0.2	0.3	0.2	0.3
	V_{zero} (%)	0.2	0.4	0.3	0.5
	I_{neg} (%)	0.3	0.6	1.1	4.5
	I_{zero} (%)	0.2	0.4	0.3	0.2
Line–neutral imbalanced load	CF	1.54	1.43	2.21	3.43
	VR (%)	12.6~30.8	0.41~0.83	7.43~19.0	0.17~0.57
	THD_V (%)	6.3~12.0	0.7~0.9	7.4~16.2	0.9~2.6
	V_{neg} (%)	5.9	0.3	3.8	0.3
	V_{zero} (%)	24.0	0.8	15.3	0.6
	I_{neg} (%)	100	100	100	100
	I_{zero} (%)	100	100	100	100
Line–line imbalanced load	CF	1.48	1.43	2.30	3.38
	VR (%)	1.4~14.3	0.4~0.7	0.25~12.3	0.08~0.25
	THD_V (%)	3.6~6.9	0.7~0.9	3.6~11.5	0.8~1.9
	V_{neg} (%)	11.0	0.2	7.4	0.3
	V_{zero} (%)	4.9	0.4	4.5	0.4
	I_{neg} (%)	100	100	100	100
	I_{zero} (%)	0.2	0.2	0.2	0.1

Fig. 15 shows the closed-loop-controlled FLI-PS performance under nonlinear balanced rated load. For this case, the FLI-PS produces output voltages with THD_V of 1.8% and VR of 0.33% with load-current CF of 2.6. Thus, the experimental results verify the computer simulations, and as predicted in the computer simulations, the experimental performance of the PS is superior to the commercial state-of-the-art (1%). Detailed steady-state performance results for various (particularly imbalanced) loading conditions are given in Table II. According to the table, for extreme load-current imbalances, the output voltages remain well balanced (for all load conditions, $V_{\text{neg}} < 1\%$ and $V_{\text{zero}} < 1\%$) and THD_V remains low (for linear load, $THD_V < 1\%$; for nonlinear load, $THD_V < 3\%$). For all cases, VR is less than 1%, illustrating the superior performance of the proposed control method.

The dynamic performance of the FLI-PS is tested in the laboratory under the same resistive loading condition as the simulations. The voltage dip, settling time, and the lost volt–seconds

TABLE III
DYNAMIC PERFORMANCE CHARACTERISTICS (LOADING)

Controller	Δt (ms)	ΔV (V)	∫vdt (V·ms)
Open-loop (only V_{ffw} active)	1.65	85	70.13
Fund. freq. res. filter added	1.58	90	71.20
Harmonics freq. res. filters added	1.05	90	47.25
Prop. cont. loop (K_{pv}) added	0.88	88	38.72
K_{ad} added and gains increased	0.63	68	21.50

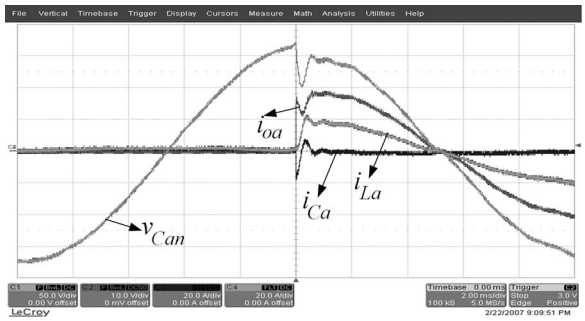

Fig. 16. Output voltage, load current (scale: ×2), inductor current, and capacitor current transients (scales: 50 V/div, 20 A/div, 2 ms/div).

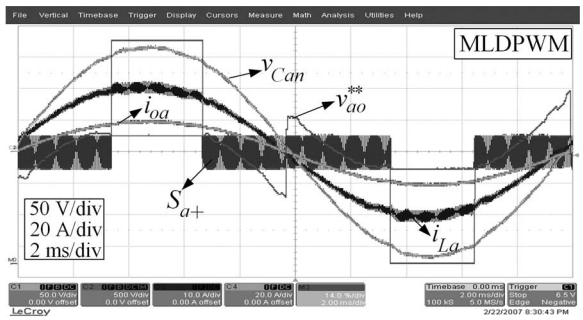

Fig. 17. Output voltage, modulation/switch logic signals, load current, and inductor current (scale: ×2) under linear balanced load.

are measured and listed in Table III. Both open- and closed-loop tests are conducted. The voltage dip is mainly improved by the active-damping loop, while all the controllers contribute to the improvement in the settling time practically equally. With all the controllers being active (the last line on Table III), the best dynamic response is obtained. The loading transient waveforms for this case are shown in Fig. 16. The waveforms are in high correlation with the simulation results, indicating the satisfactory performance of the control system.

As a final experiment, for balanced, resistive rated-load, closed-loop, and steady-state operation, the inverter and load current, output voltage, and modulation/switch logic signal waveforms are shown in Fig. 17 for MLDPWM. The waveforms are in correlation with the computer simulation results of Fig. 12. As shown by computer simulations, for the nonlinear and imbalanced loads, MLDPWM has superior performance compared to DPWM1 in terms of switching count (losses). For linear resistive line-to-neutral imbalanced rated load, MLDPWM and DPWM1 method waveforms are shown in Fig. 18. For MLDPWM, switching of the loaded phase ceases longer than 120°, while for DPWM1, it ceases for approximately 120° as expected. In addition, there is no significant difference between the PWM current ripple of the two cases. This shows that

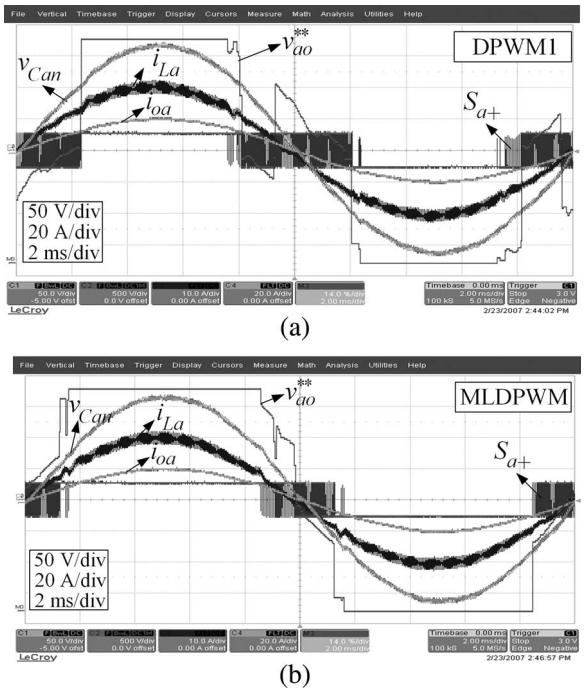

Fig. 18. Output voltage, modulation/switch logic signals, load current, and inductor current (scale: $\times 2$) under linear line-to-neutral imbalanced load.

MLDPWM is superior to DPWM1 and GDPWM [34] in terms of switching losses. In Fig. 18(a) and (b), the discrepancies on the modulation waves near the edges are due to the DSP-chip PWM-module duty-cycle updating constraints.

MLDPWM is not strictly limited to the FLI-PS but can also be beneficial to other FLI applications such as grid-connected voltage source converter, transformerless UPS, etc., applications where imbalanced line/load conditions are not unusual.

VI. Conclusion

Employing a simple and easy to implement all-scalar-control and PWM approach for the FLI-based three-phase transformerless four-wire PS, high steady-state and dynamic performance could be obtained. The resonant-filter controllers provide precise output-voltage regulation and low harmonic distortion under severe operating conditions such as high-crest-factor nonlinear load and imbalanced load. Better than 1% voltage regulation and 3% voltage THD are obtained. Utilizing the inverter zero-state partitioning, a generalized form of scalar PWM for the FLI is developed. A novel MLDPWM method, which provides minimum switching losses under all loading conditions (including imbalance), is developed. MLDPWM has at least 25.2% less switching loss than the conventional DPWM method. The scalar-control and PWM methods are proven by means of theory, simulations, and thorough laboratory experiments of a 5-kVA PS.

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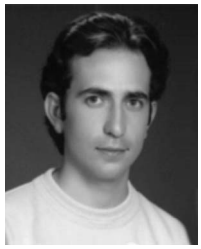

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